THE INVENTION CLAIMED IS:

1. A method of forming an integrated circuit comprising:
providing a semiconductor substrate;
forming a gate dielectric on the semiconductor substrate;
forming a gate over the gate dielectric;
forming source/drain junctions in the semiconductor substrate;
forming ultra-uniform silicides on the source/drain junctions;
depositing a dielectric layer above the semiconductor substrate; and
forming contacts in the dielectric layer to the ultra-uniform silicides.

2. The method as claimed in claim 1 wherein:
forming the ultra-uniform silicides uses a very low power deposition technique using a power level below 500 watts direct current.

3. The method as claimed in claim 1 wherein:
forming the ultra-uniform silicides uses an extra slow rate of deposition of a silicide metal below 7.0 Å per second.

4. The method as claimed in claim 1 wherein:
forming the ultra-uniform silicides forms an ultra-thin thickness of a silicide metal of not more than 50 Å thick.

5. The method as claimed in claim 1 wherein:
depositing the dielectric layer deposits a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

6. The method as claimed in claim 1 wherein:
forming the contacts to the ultra-uniform silicides uses materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

7. A method of forming an integrated circuit comprising:
providing a silicon substrate;
forming a gate oxide on the silicon substrate;
forming a polysilicon gate over the gate oxide;
forming source/drain junctions in the silicon substrate;

forming an ultra-uniform nickel silicide having no variations in thickness greater than 3% of the overall thickness on the source/drain junctions and on the gate;

depositing a dielectric layer above the silicon substrate; and

forming contacts in the dielectric layer to the ultra-uniform nickel silicide.

8. The method as claimed in claim 7 wherein:

forming the ultra-uniform nickel silicide uses a vapor deposition using a power level below 400 watts direct current.

9. The method as claimed in claim 7 wherein:

forming the ultra-uniform nickel silicide uses an extra slow rate of deposition of nickel below 6.8 Å per second; and

additionally comprising:

an annealing of the nickel to the ultra-uniform nickel silicide.

10. The method as claimed in claim 7 wherein:

forming the ultra-uniform nickel silicide uses an ultra-thin thickness of nickel of not more than 50 Å thickness.

11. The method as claimed in claim 7 wherein:

depositing the dielectric layer deposits a dielectric material having a dielectric constant below 4.2.

12. The method as claimed in claim 7 wherein:

forming the contacts to the ultra-uniform silicides uses materials selected from a group consisting of tantalum, titanium, tungsten copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

13. An integrated circuit comprising:

a semiconductor substrate having source/drain junctions;

a gate dielectric on the semiconductor substrate;

a gate over the gate dielectric;

ultra-uniform silicides on the source/drain junctions;

a dielectric layer above the semiconductor substrate; and

contacts in the dielectric layer to the ultra-uniform silicides.

14. The integrated circuit as claimed in claim 13 wherein:

the ultra-uniform silicides is an ultra-thin thickness of a silicide metal of not more than 50 Å thick.

15. The integrated circuit as claimed in claim 13 wherein:

the dielectric layer deposits a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

16. The integrated circuit as claimed in claim 13 wherein:

the contacts to the ultra-uniform silicides are of materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

17. An integrated circuit comprising:

a silicon substrate having source/drain junctions;

a gate oxide on the silicon substrate;

a polysilicon gate over the gate oxide;

an ultra-uniform nickel silicide on the source/drain junctions and the polysilicon gate, the ultra-uniform nickel silicide having no variations in thickness greater than 3% of the overall thickness;

a dielectric layer above the silicon substrate; and

contacts in the dielectric layer to the ultra-uniform nickel silicide.

18. The integrated circuit as claimed in claim 17 wherein:

the ultra-uniform nickel silicide is an ultra-thin thickness of a silicide metal of not more than 50 Å thickness.

19. The integrated circuit as claimed in claim 17 wherein:

the dielectric layer is a dielectric material having a dielectric constant below 4.2.

20. The integrated circuit as claimed in claim 17 wherein:

the contacts to the ultra-uniform silicides are of materials selected from a group consisting of tantalum, titanium, tungsten copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.